FIG. 1

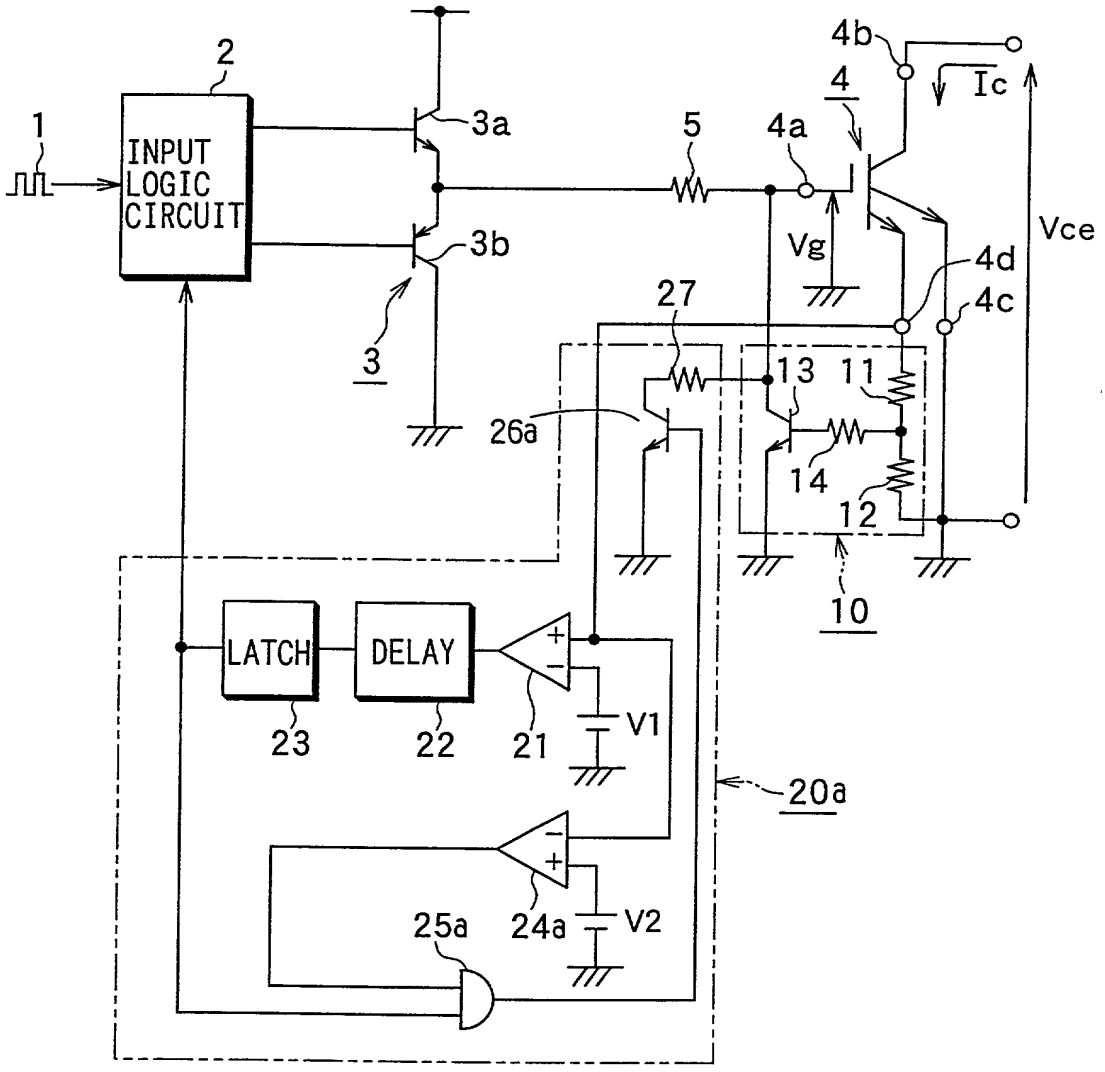

1
2
INPUT
LOGIC
CIRCUIT
3a
3b
3
5
4a
4
4b
Ic
Vg
Vce
4d
4c
27
13
11
14
12
10
26a
LATCH
DELAY
23
22
21
V1
20a
25a
24a
V2

FIG. 2A

Ic

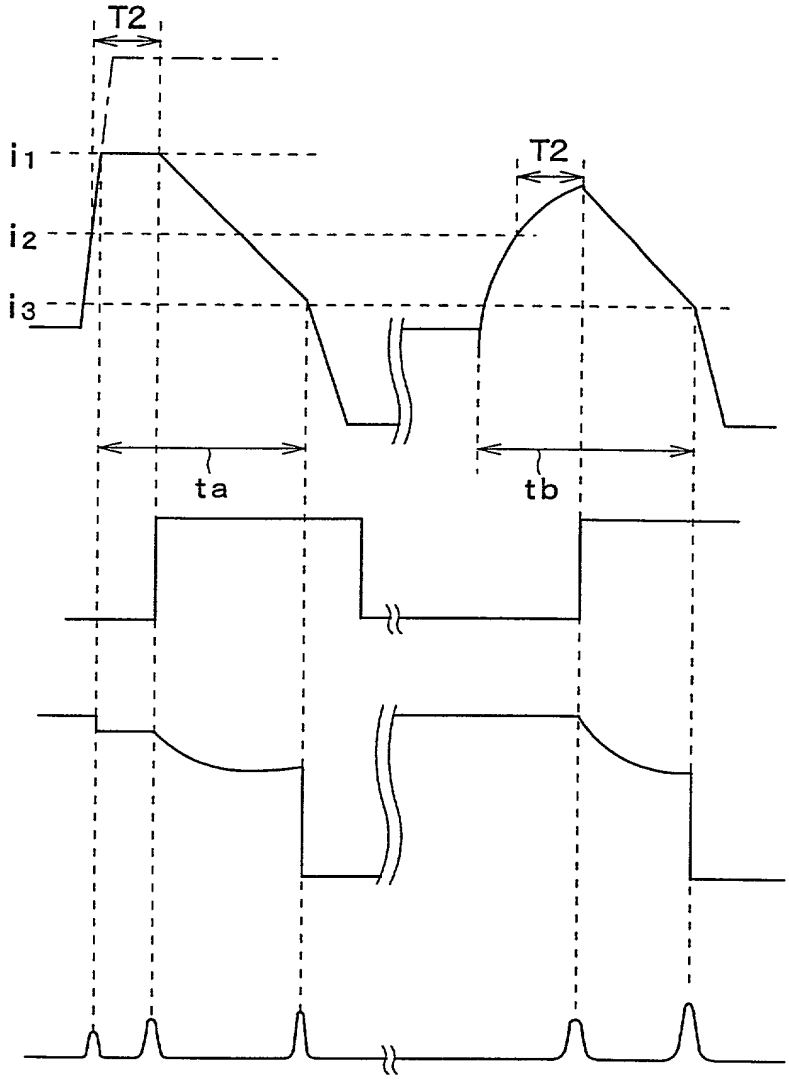


FIG. 2B

OUTPUT OF
LATCH CIRCUIT

FIG. 2C

Vg

FIG. 2D

Vce

FIG. 3

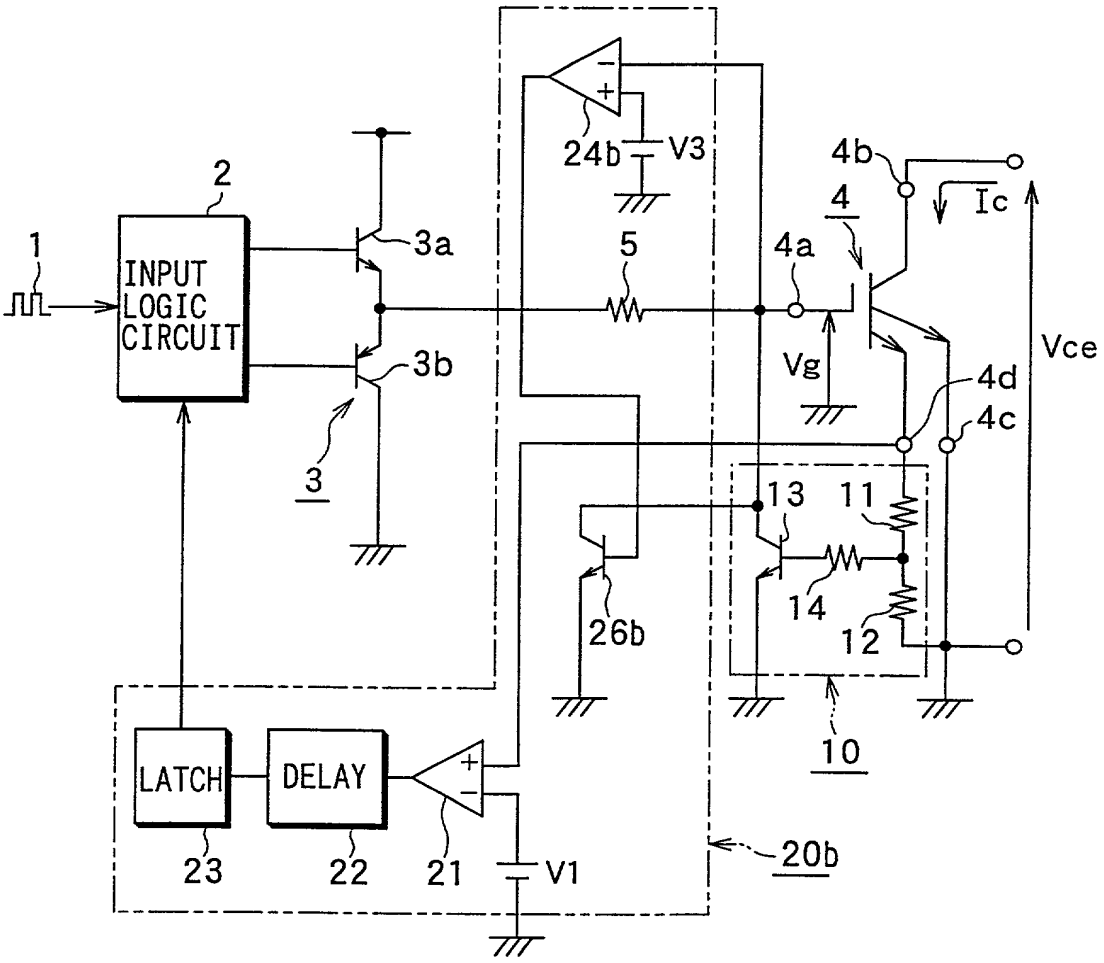

1
2
INPUT
LOGIC
CIRCUIT
3a
3b
3
24b
V3
5
4b
4
Ic
4a
Vg
Vce
4d
4c
13
11
14
12
26b
10
LATCH
DELAY
23
22
21
V1
20b

FIG. 4

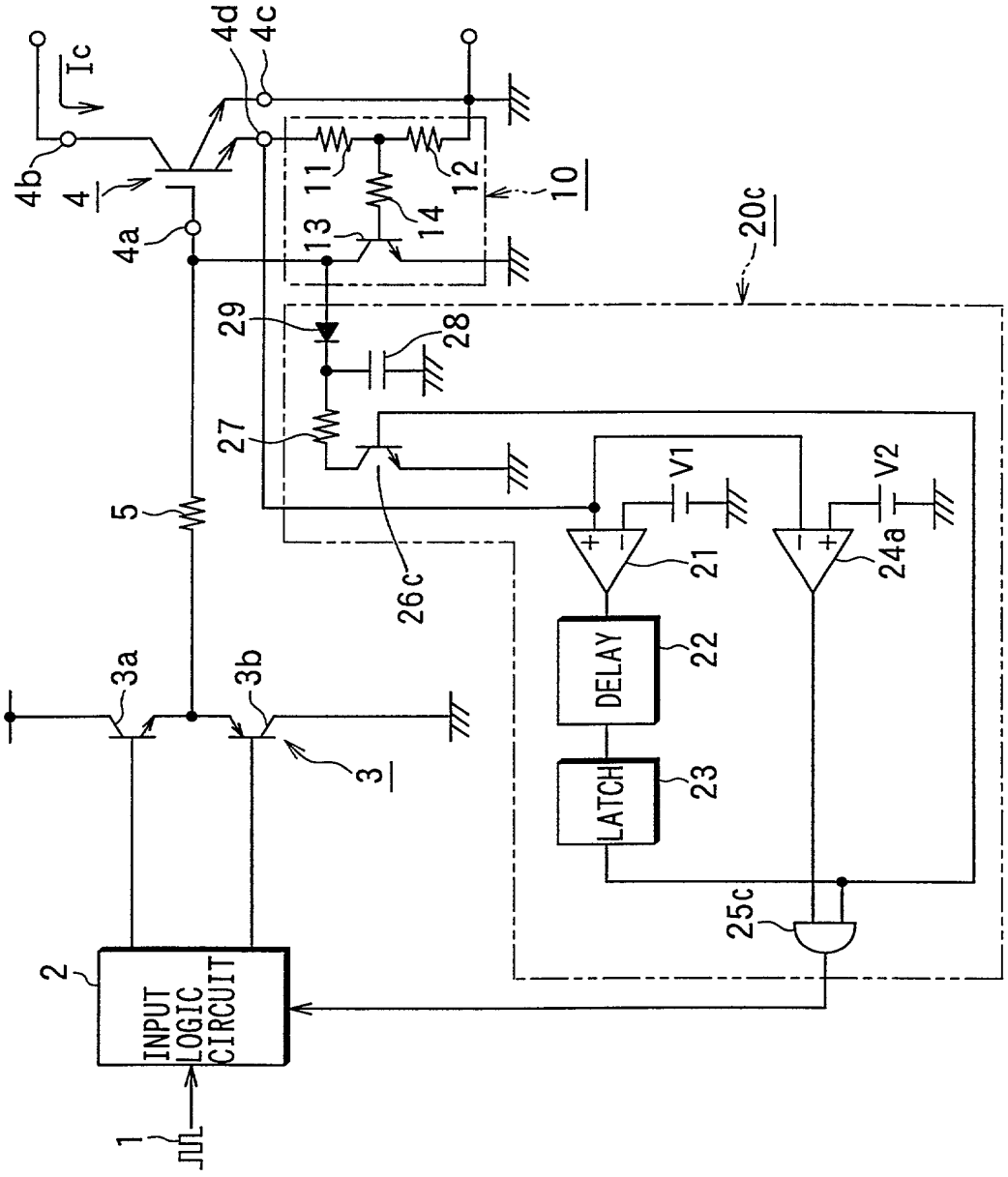

Ic
4d
4c
4b
4
4a
10
11
12
13
14
20c
29
28
27
5
26c
V1
V2
21
24a
DELAY
22
LATCH
23
25c
3a
3b
3
2
INPUT LOGIC CIRCUIT
1

FIG. 5A

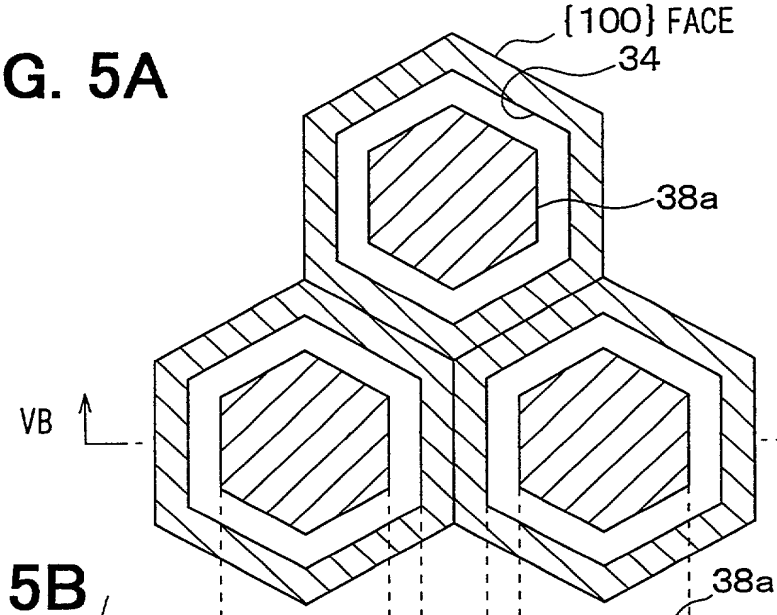

{100} FACE
34
38a
VB
VB

FIG. 5B

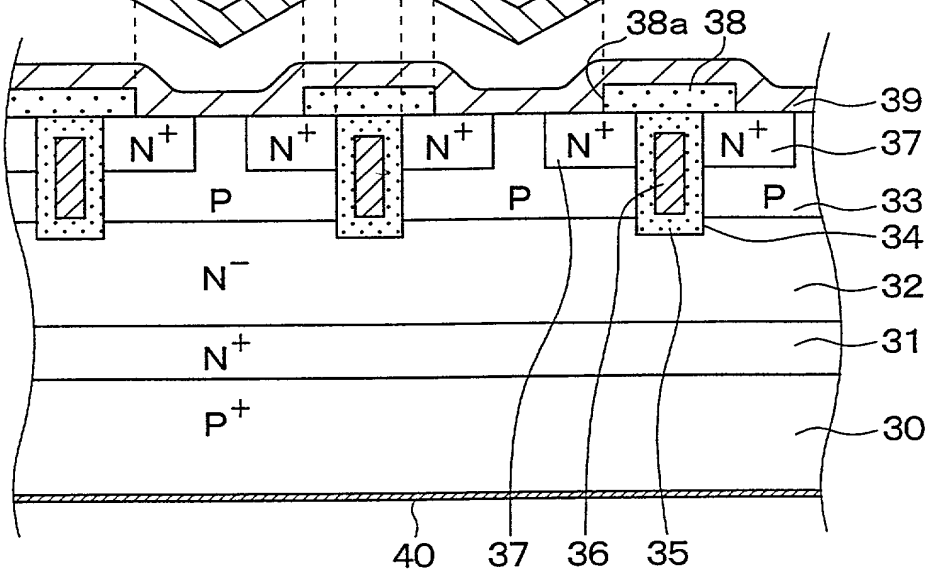

38a 38
39
N+
N+
N+
N+
N+
37
P
P
P
33
34
N−
32
N+
31
P+
30
40
37
36
35

FIG. 6

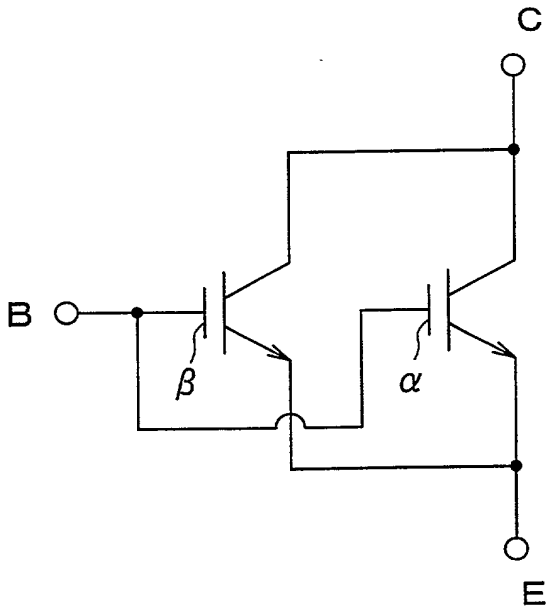


FIG. 7

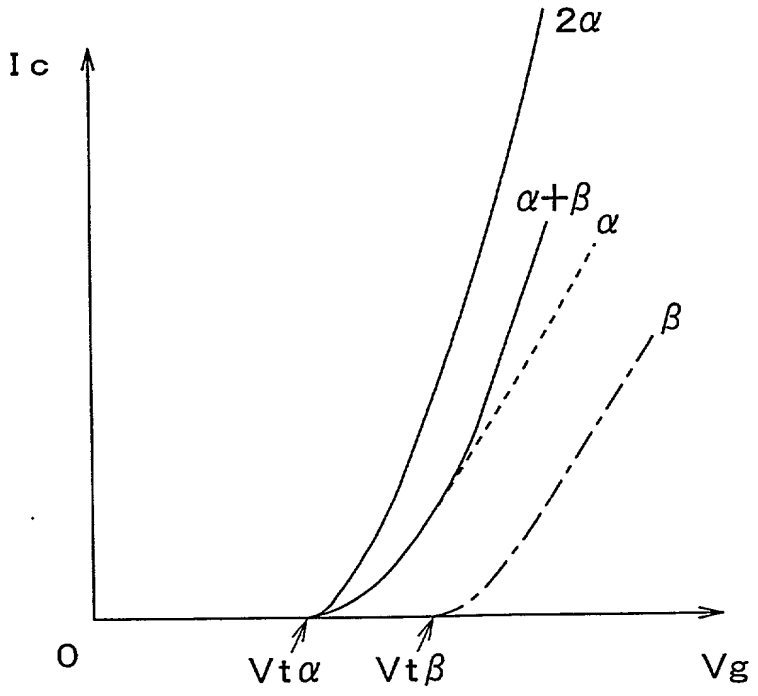


FIG. 8

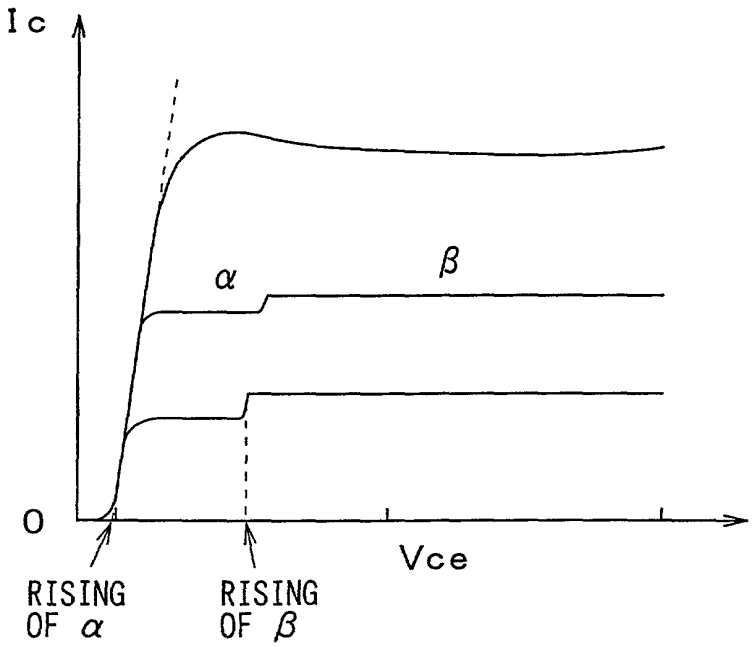


FIG. 9A

FIG. 9B

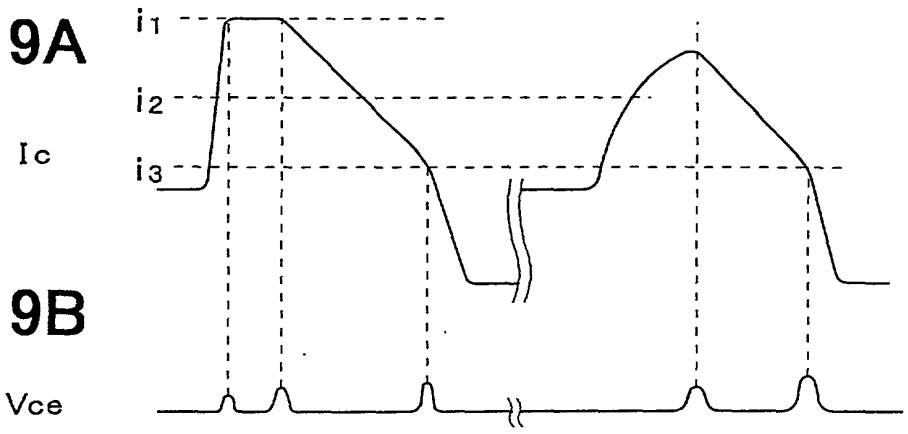


FIG. 10A

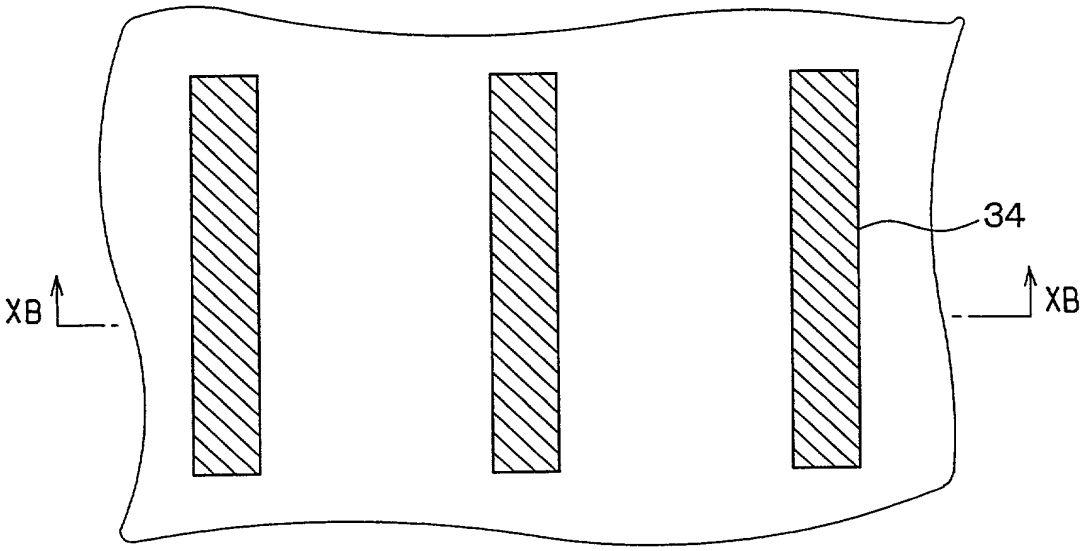


FIG. 10B

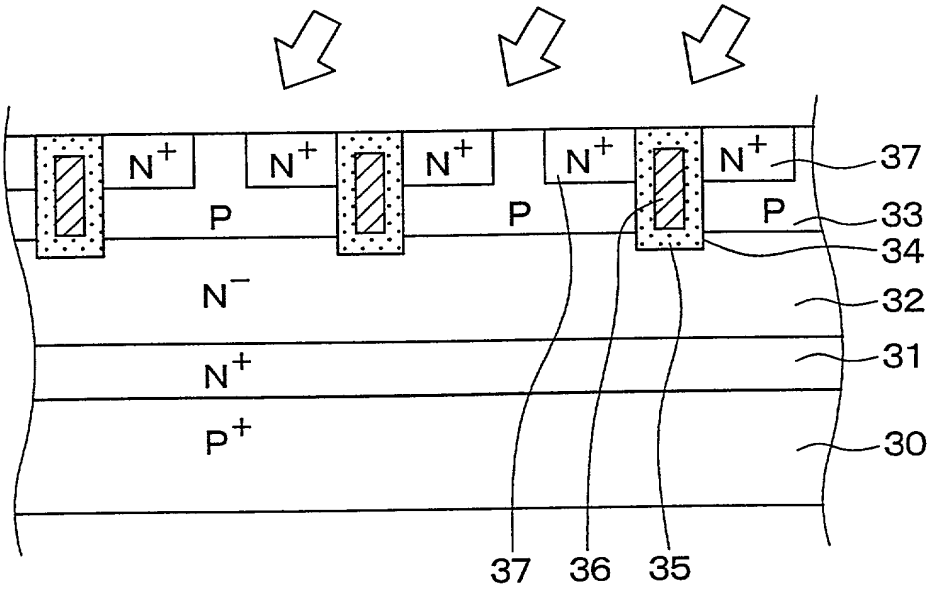


FIG. 11
PRIOR ART

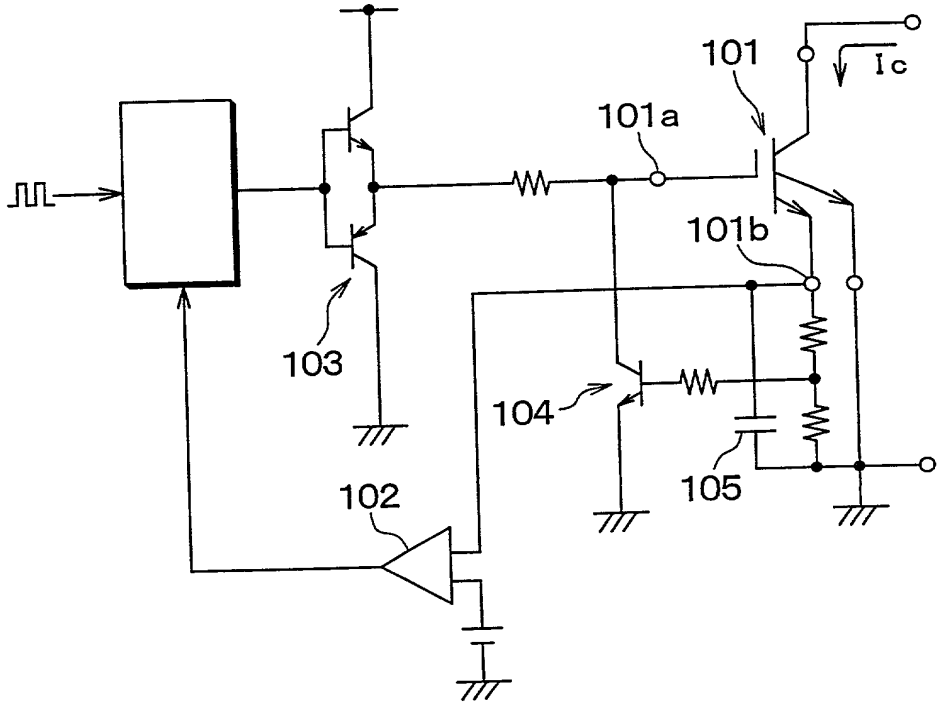


FIG. 12
PRIOR ART

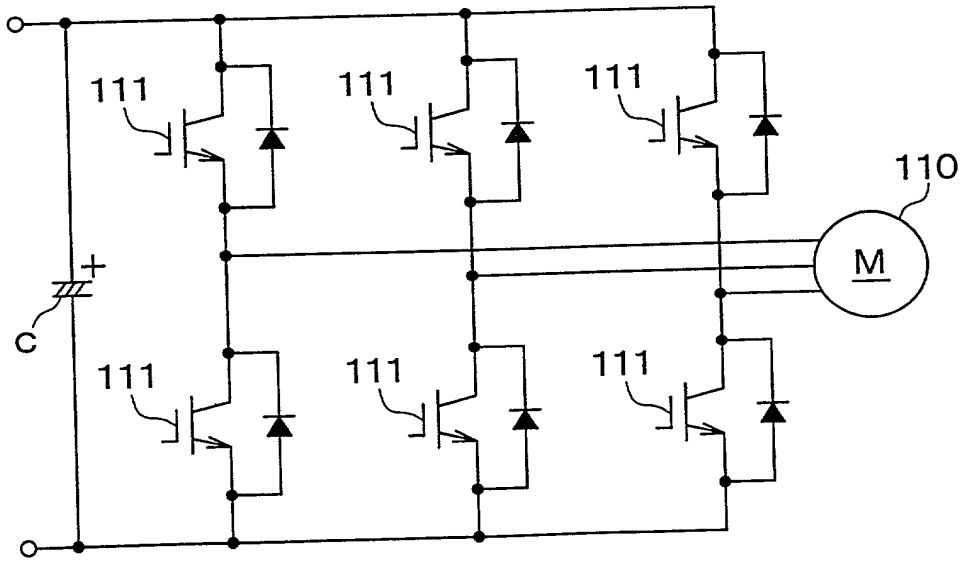


FIG. 13

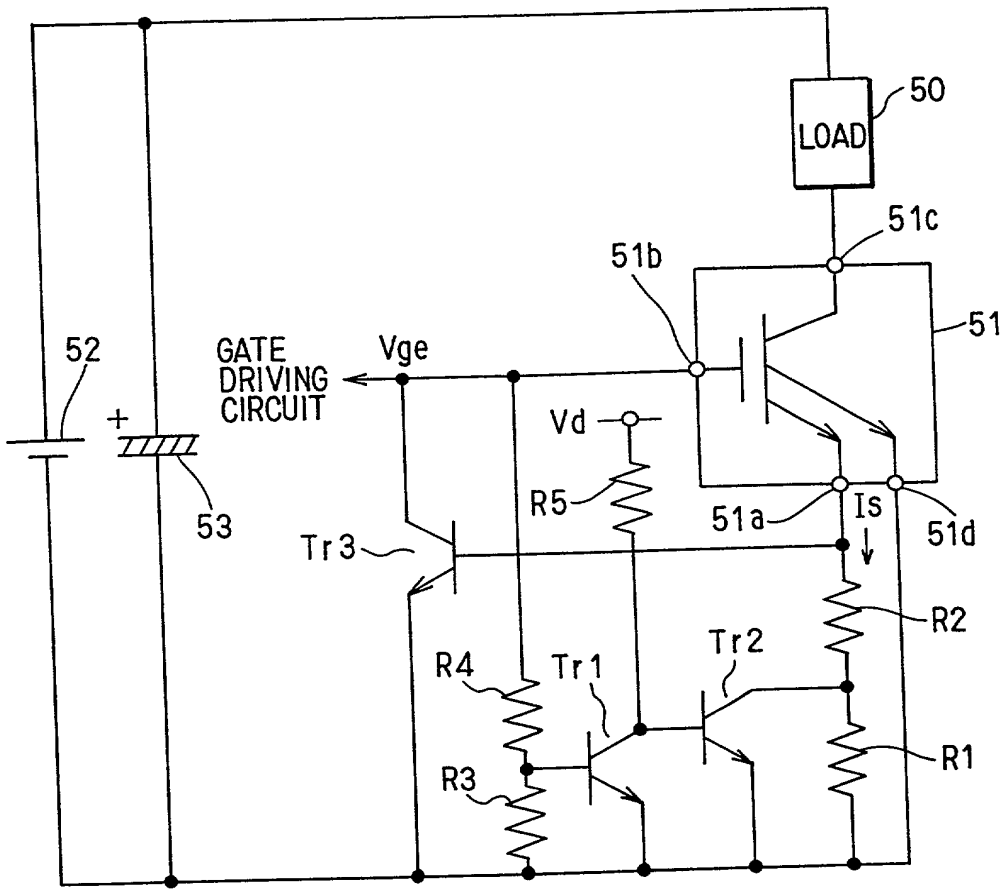

LOAD
50
51c
51b
51
52
GATE
DRIVING
CIRCUIT
Vge
Vd
+
53
R5
51a
Is
51d
Tr3
R2
R4
Tr1
Tr2
R1
R3

FIG. 14

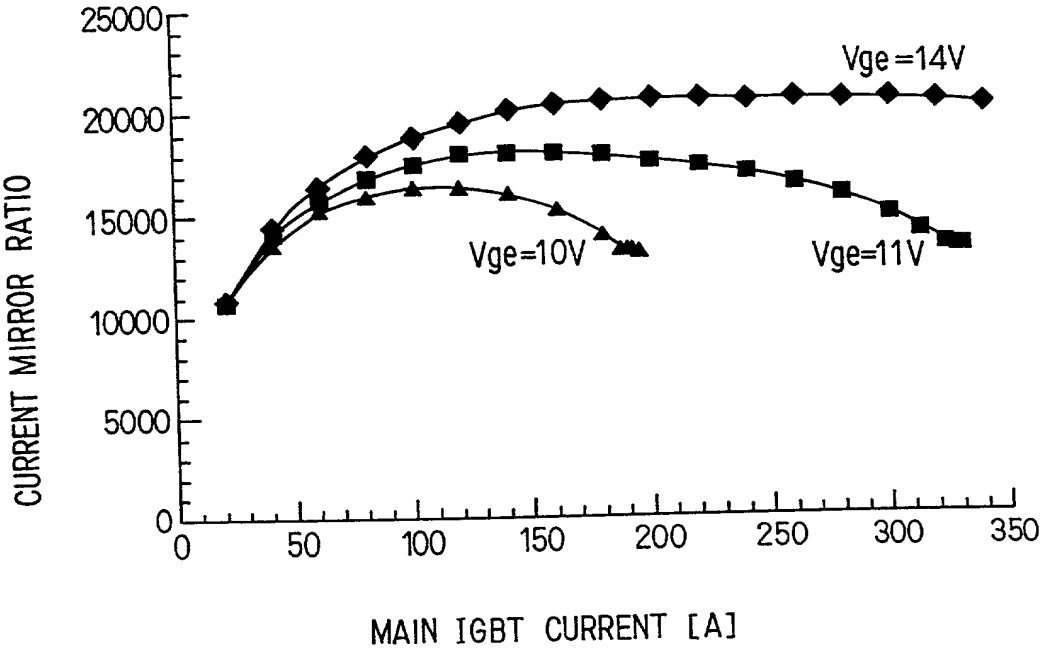

CURRENT MIRROR RATIO
25000
20000
15000
10000
5000
0
0
50
100
150
200
250
300
350
Vge=14V
Vge=10V
Vge=11V
MAIN IGBT CURRENT [A]

FIG. 15

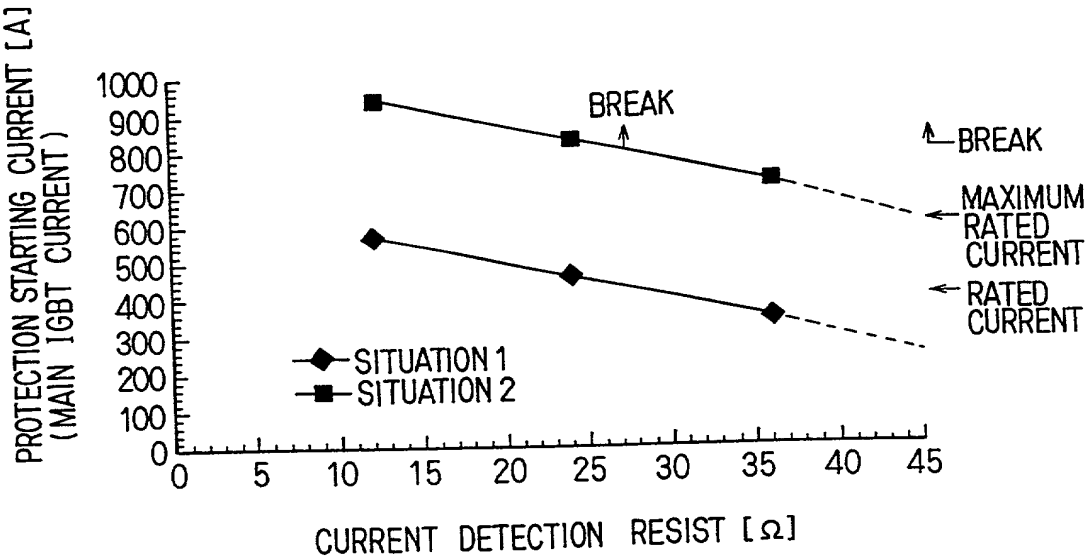
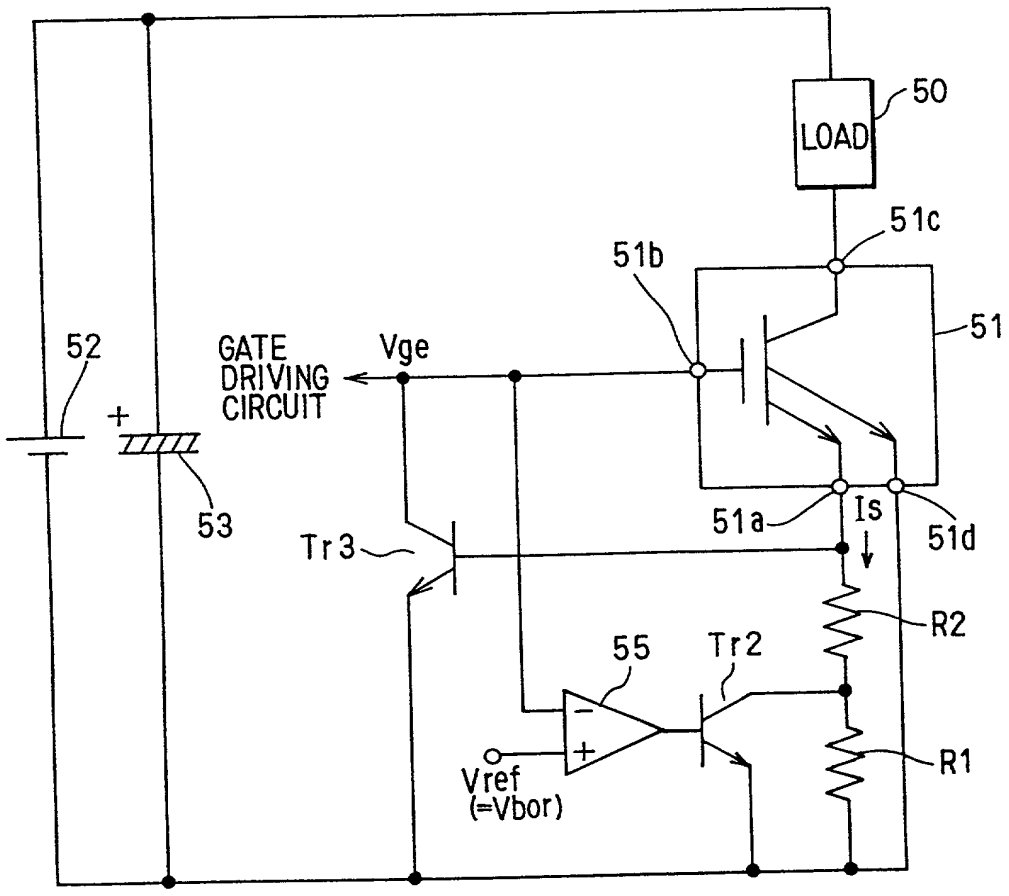

PROTECTION STARTING CURRENT [A]
(MAIN IGBT CURRENT)
1000
900
800
700
600
500
400
300
200
100
0
0
5
10
15
20
25
30
35
40
45
BREAK
BREAK
MAXIMUM RATED CURRENT
RATED CURRENT
SITUATION 1
SITUATION 2
CURRENT DETECTION RESIST [Ω]

FIG. 16


LOAD
50
51c
51b
51
52
GATE
DRIVING
CIRCUIT
Vge
+
53
Tr3
51a
Is
51d
R2
55
Tr2
R1
Vref
(=Vbor)